REMARKS

In the Final Office Action, the Examiner noted that claims 1-30 are pending in the application and that claims 1-15 are rejected. Claims 16-30 have been withdrawn from consideration. By this response, claim 1 is amended and claims 15-30 are cancelled. In view of the above amendments and the following discussion, Applicants submit that none of the claims now pending in the application are obvious under the provisions of 35 U.S.C. §103. Thus, Applicants believe that all of these claims are now in condition for allowance.

REJECTION OF CLAIMS UNDER 35 U.S.C. §103

A. Claims 1-14

The Examiner rejected claims 1-14 as being unpatentable over Chong (U.S. Patent 6,624,489, issued September 23, 2003) in view of Buynoski (U.S. Patent 6,518,113, issued February 11, 2003). The rejection is respectfully traversed.

Chong teaches formation of silicided shallow junctions using implant through metal technology and laser annealing process. The method taught by Chong forms a gate transistor comprising a silicide layer, heavily doped layer, polysilicon layer, and a gate oxide layer, in that order. (See Chong, Fig. 11, Col. 5, Line 44 - Col. 6, Line 15.)

Buynoski teaches doping of thin amorphous silicon work function control layers of MOS gate electrodes. Buynoski's method applies to in-laid ("damascene") gates. (See Buynoski, Col. 1, Lines13-15.) Both methods taught by Buynoski involve forming the source drain regions, forming a doped polysilicon layer over a thin gate insulator layer and then filling a void with a metal contact (i.e. the "damascene" method). (See Buynoski, Fig. 7(A), Fig. 16(A); Col. 12, Line 43 - Col. 13, Line 21.)

The cited references, either singly or in any permissible combination, do not teach, suggest, or otherwise render obvious Applicants' invention recited in claim 1. Namely, the combination of Chong and Buynoski does not teach or suggest siliciding the polysilicon gate electrode to form a silicide and at least one monolayer of the at least one dopant at an interface between the gate dielectric layer and the silicide. Specifically, Applicants' independent claim 1 positively recites:

> A method of fabricating a complementary metal oxide semiconductor (CMOS) field effect transistor, comprising the steps of:
> (a) providing a substrate;
> (b) providing on said substrate a polysilicon layer formed upon a gate dielectric layer of a gate structure of the transistor;
> (c) doping the polysilicon layer using at least one dopant;
> (d) forming a polysilicon gate electrode of the gate structure;
> (e) depositing on the polysilicon gate electrode at least one of a metal and an alloy; and
> (f) siliciding the polysilicon gate electrode to form a silicide and at least one monolayer of the at least one dopant at an interface between the gate dielectric layer and the silicide.

(Emphasis added). Claim 1 has been amended to include substantial features of claim 15. which has been cancelled. Applicants contend that the amendment places claims 1-14 in condition for allowance or, alternatively, in better form for appeal. As such, Applicants respectfully request entry of the amendment.

First, Buynoski does not teach or suggest a silicide gate electrode. Rather, the gate electrode in Buynoski is metal. Second, Chong does not teach or suggest at least one monolayer at an interface between the gate dielectric layer and the silicide. Rather, the silicide layer of Chong is separated from the gate oxide layer by a polysilicon layer. The polysilicon layer of Chong does not teach or suggest at least one monolayer of at least one dopant. That is, in Chong, a shallow silicide junction is formed such that a portion of the polysilicon remains after the process. Chong states:

> The dopant diffusion is, therefore, limited to the previously defined amorphous region (22). The amorphous Si layer then recrystallizes from the underlying substrate at a high re-growth velocity such that the metal atoms do not diffuse through the entire depth of the melt. In this way, shallow junctions and silicides can be formed simultaneously.

(Chong, col. 6, lines 5-15). Accordingly, the process of Chong does not push the dopants in the polysilicon layer to form monolayer(s) at the interface of the gate oxide.

In Applicants' invention, the at least one monolayer at the interface between the gate dielectric layer and the silicide advantageously allows for an improved work function and improved electron mobility. (See Applicants' specification, ¶0028). Neither Buynoski nor Chong achieves such advantages. Since neither Buynoski nor Chong teaches or suggests siliciding the polysilicon gate electrode to form a silicide and at least one monolayer of the at least one dopant at an interface between the gate

dielectric layer and the silicide, no conceivable combination of Buynoski and Chong renders obvious Applicants' invention recited in claim 1.

Furthermore, in rejecting claim 15, the Examiner stated that Vaidya (Vaidya et al., "Effect of Dopant Implantation on the properties of $TaSi_2$/poly-Si composites," J. Vac. Sci. Technol., May/June 1985) teaches an annealing process where at least one monolayer of dopant is formed at an interface of a dielectric and silicide. Vaidya generally discloses the effect of dopant implantation and redistribution on the properties of $TaSi_2$/poly-Si structures. Vaidya does not teach or suggest siliciding a polysilicon gate electrode to form a silicide and at least one monolayer of the at least one dopant at an interface between the gate dielectric layer and the silicide. Moreover, there is no teaching or suggestion to combine Vaidya with Buynoski and Chong. Since Chong explicitly teaches the use and advantages of a shallow silicide junction, Chong teaches away from any modification thereof that would form at least one monolayer at the interface of the gate oxide.

For these reasons, Applicants contend that the invention of claim 1 is patentable over the cited references and, as such, fully satisfies the requirements of 35 U.S.C. §103. Claims 2-14 depend, either directly or indirectly, from claim 1 and recite additional features therefor. Since the combination of the cited references does not render obvious Applicants' invention as recited in claim 1, dependent claims 2-14 are also nonobvious and are allowable.

B. Claim 15

The Examiner rejected claim 15 as being unpatentable over Chong and Buynoski in further view of Vaidya. Applicants have cancelled claim 15. Accordingly, the rejection of claim 15 is moot.

Conclusion

Thus, the Applicants submit that all of these claims now fully satisfy the requirement of 35 U.S.C. §103. Consequently, the Applicants believe that all these

claims are presently in condition for allowance. Accordingly, both reconsideration of this application and its swift passage to issue are earnestly solicited.

If, however, the Examiner believes that there are any unresolved issues requiring the maintenance of any final action in any of the claims now pending in the application, it is requested that the Examiner telephone Mr. Kin-Wah Tong, Esq. at (732) 530-9404 so that appropriate arrangements can be made for resolving such issues as expeditiously as possible.

Respectfully submitted,

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